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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/467,992	12/20/1999	LEONARD FORBES	303.389US2	3099

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EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/467,992	FORBES ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-19,22,23,25-27,29,31,32,34-37,39-48,50,52 and 53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-19,22,23,25-27,29,31,32,34-37,39-48,50,52,53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 17 thru 19, 22, 23, 25, 31, 32, 34, 37, 39, 41 thru 46, 48, 52, and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh 4,920,389 in view of Kanetaki et al. 4,906,590. Itoh discloses (see, for example, FIG_ 8(k)) a memory cell array structure comprising memory cells wherein an individual memory cell comprises bit lines 222, word lines 234, a low electric resistance region (first source/drain region) 232, high electric resistance semiconductor layer (body region) 204, low electric resistance semiconductor layer (second source/drain region) 202, highly electroconductive layer (second plate) 216 and gate 234. In column 13, lines 18-32, Itoh discloses the low electric resistance semiconductor layer 202 serving as a first electrode (first plate) of a capacitor as well as a source region. In column 10, lines 31-41, Itoh discloses the highly electroconductive layer comprising polycrystalline silicon. Itoh does not disclose an etch-roughened surface. However, Kanetaki discloses (see, for example, FIG. 2) a trench capacitor containing two plurality of hollows (roughened surfaces). In column 1, lines 11- *, Kanetaki states that the plurality of hollows increases the electrode area without increasing the planar area. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include the plurality of hollows (roughened surfaces) in Itoh's invention in order to increase the electrode area without increasing the planar area.

Regarding claim 52 and the limitation "word line", see FIG_8(k) wherein Itoh discloses a gate electrode (word line) 234.

Regarding claim 53 and the limitation "plurality of bit lines", see FIG_8(k) wherein Itoh discloses bit lines 222.

3. Claims 26, 27, 29, 35, 36, 40, 47, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh '389 in view of Kanetaki et al. '590 as applied to claims 17-19, 22, 23, 25, 31, 32, 34, 37, 39, 41 thru 46, 48, 52, and 53 above, and further in view of Wahlstrom 5,396,452. Itoh in view of Kanetaki does not disclose a row decoder and column decoder so as to selectively access the cells of an array. However, Wahlstrom discloses (see, for example, FIG. 2) a dynamic random access memory comprising memory cells arranged in an array wherein word lines (WL) are arranged orthogonal to bit lines (BL). In FIG. 1, Wahlstrom shows a row decoder and a column decoder which access the memory cells according to the row and column addresses applied. It would have been obvious to one of ordinary skill in the art at the time of invention to have a column and row decoder in order to form a memory cell array wherein the individual memory cells may be accessed easily.

Response to Arguments

4. Applicant's arguments with respect to claims 17-19, 22, 23, 25-27, 29, 31, 32, 34-37, 39-48, 50, 52, and 53 have been considered but are moot in view of the new ground(s) of rejection.

Regarding applicant's argument on page 13, first paragraph that Itoh and Kanetaki et al. does not disclose a second plate that is formed in a trench that "surrounds the first plate" and a

gate adjacent to the body region and "the gate being vertically aligned with the second plate", this argument is not persuasive. In FIG_8(k), Itoh discloses the second plate 216 which surrounds the entire edge of first plate 202 and a gate 234 adjacent to the body region 204. The gate is vertically aligned with second plate 216 in that they have a vertical relationship with each other and separated by a vertical distance even though they are not directly above each other.

Regarding applicant's argument on page 13, fourth paragraph that Itoh and Kanetaki et al. does not disclose "the first plate surrounds at least a portion of the second plate" and "a gate adjacent to the body region and the gate being vertically aligned with the polysilicon second plate", this argument is not persuasive. In FIG_8(k), Itoh discloses the first plate 202 which surrounds the entire edge of second plate 216 and a gate 234 adjacent to the body region 204. The gate is vertically aligned with second plate 216 in that they have a vertical relationship with each other and separated by a vertical distance even though they are not directly above each other.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Eugene Lee
January 4, 2005